SIMULATION RESULTS OF CURRENT FED INTERLINE POWER FLOW CONTROLLER USING SIMULINK

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Abstract: Interline Power Flow Controllers (IPFC) have been used to enhance and optimize the use of transmission facilities, under the concept of a Flexible AC Transmission System (FACTS). The main objectives of FACTS are to increase the useable transmission capacity of lines and control power flow over designated transmission routes. Interline Power Flow Controllers are the classical-series or series-parallel filters applied to given number of independent lines with common, DC element. The simulation results of current fed IPFC are presented.

Keywords: IPFC, FACTS, SSSC, Simulink, TCSC.

1. INTRODUCTION

FACTS are one aspect of the power electronics revolution that is taking place in all areas of electrical energy. A variety of power semiconductor devices not only offer the advantage of high speed and reliability of switching but , more importantly, the opportunity offered by a variety of innovative circuits concepts based on these power devices enhance the value of electrical energy.

The control of an AC power system in real time is involved because power flow is a function of the transmission line impedence, the magnitude of the sending end voltages, and the phase angle between the voltages. It is generally understood that AC transmission system could not be controlled fast enough to handle dynamic system conditions.

In recent years, the development of semiconductor technology has led to the use of power electronics in electrical power devices. The advantages of these so called Flexible AC Transmission System (FACTS) devices are primarily rapid response and enhanced flexibility. Flexible AC Transmission Systems (FACTS) devices are integrated in power system to control power flow, increase transmission line stability limit and improve the security of transmission system. FACTS controllers are used to enhance the system flexibility and increase system loadability.

2. INTERLINE POWER FLOW CONTROLLER (IPFC)

The Interline power flow Controller provides (IPFC), in addition to the facility for independently controllable reactive (series) compensation of each individual line, a capability to directly transfer or exchange real power between the compensated lines. This is achieved by coupling the series connected VSCs in individual lines on the DC side, by connecting all the DC capacitors of individual converters in parallel. Since all the series converters

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are located inside the substation in close proximity, this is feasible.

An IPFC with two converters compensating two lines (shown in Fig.1) is similar to a UPFC in that the magnitude and phase angle of the injected voltage in the prime system (which is also a series converter in the second line). The basic difference with a UPFC is that the support system in the later case is the shunt converter instead of a series converter. The series converter associated with the n prime system (of one IPFC) is termed as the master converter while the series converter associated with the support system is termed as the slave converter. The master converter controls both active and reactive voltage (within limits) while the slave converter controls the DC voltage (across the capacitor) and the reactive voltage magnitude.

For the system shown in Figure.1, we can express the received power and the injected reactive power at the receiving end of the prime line (# 1) by the following expressions.

$$P_1 = P_{10} + \frac{VV_{p1}}{X_1}\sin\left(\frac{\delta_1}{2} - \phi_1\right) + \frac{VV_{r1}}{X_1}\cos\left(\frac{\delta_1}{2} - \phi_1\right)$$

$$Q_1 = Q_{10} - \frac{VV_{p1}}{X_1}\cos\left(\frac{\delta_1}{2} - \phi_1\right) + \frac{VV_{r1}}{X_1}\sin\left(\frac{\delta_1}{2} - \phi_1\right)$$

Where

$$\delta_1 = \theta_1 - \theta_2, \quad \sin\phi_1 = \frac{V_{p1}}{2V\sin\frac{\delta_1}{2}}$$

P_{10} and Q_{10} are the power and reactive power in the line 1 (at the receiving end) when both V_{p1} and V_{r1} are zero. These are given by

$$P_{10} = \frac{V^2\sin\delta_1}{X_1}, \quad Q_{10} = \frac{V^2}{X_1}(1 - \cos\delta_1)$$

Similar equations also apply to the support line (#2) except that V_{p2} is not independent. It is related to V_{p1} by the equation

$$V_{p1}I_1 + V_{p2}I_2 = 0$$

The above equation shows that V_{p2} is negative if V_{p1} is positive.

With resistance emulation, we have

$$V_{p1} = -R_1 I_1, \quad V_{p2} = -R_2 I_2$$

Substituting V_{p1} and V_{p2} value we have

$$R_1 I_1^2 = -R_2 I_2^2$$

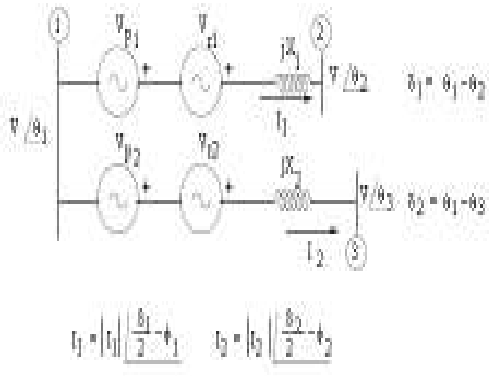

Figure.1 .Representation of IPFC

The above literature does not deal with the IPFC using current fed inverter. In the present work IPFC is proposed using current source. The interline power flow controller represents a novel concept with the objective of providing a flexible power flow control scheme for a multi line power system, in which two (or more) lines employ an SSSC for series compensation . The IPFC scheme provides, together with the independent controllable reactive compensation of each line, a capability to transfer real power between the compensated lines. this capability makes it possible to equalise both real and reactive power flow between the lines, , to transfer the power demand from over loaded lines to under loaded lines, to compensate against resistive line voltage drops and the corresponding reactive line power , and to increase the effectiveness of the compensating system for dynamic disturbances (transient stability and power oscillation damping).

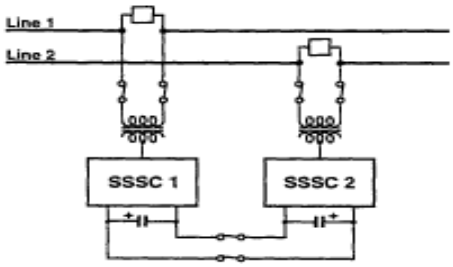

Figure.2.Elementry Interline Power Flow Controller consisting of two SSSCs operated with a common DC link.

In general, the IPFC provides a highly effective scheme for power transmission management at a multi line substation. An elementary interline power flow controller of two converter based SSSCs, connected back-to-back for real power transfer, is shown in Figure.2.Each SSSC is coupled to a different transmission line via its own series insertion transformer and is able to provide independent series reactive compensation to its own line .

The converter of each SSSC produces a

controllable AC output voltage at the fundamental frequency, which is synchronized to the voltage of the transmission line which that converter controls. The phase angle and magnitude of the two output voltages are controlled with respect to a selected bus (e.g. sending-end) voltage and the current of their own line. The injected voltage will generally have one component that is in quadrature and another that is in phase with the relevant line current.

The quadrature components provide series reactive compensation for the lines and the in -phase components define the real power absorbed from one line and generated for the other since each converter is self sufficient in generating or absorbing reactive power.

The quadrature voltage components can be independently controlled (within the converter rating) according to the reactive compensation requirements of the corresponding lines. However, since the real power exchanged by a converter and its AC terminals has to be supplied to, or absorbed from its DC terminals, the in-phase output voltage component of each of the two converters must be controlled so as to ensure a net zero real power balance at their common DC terminals. In other words, the real power compensation demand of one line must be fully supplied (or absorbed) by other lines.

The operation of the IPFC is illustrated in Figure.3. For the sake of discussion assume that line 1 is the prime line which is to be optimized for power transmission by means of independently controllable real and reactive power flow. Line 2 is assumed to have capacity to provide the real power needed for the optimization of the power flow in Figure shows the single line power system 1, with sending end bus providing power for Line 1(represented by line inductance X_1), the receiving end bus, and the controllable AC voltage source representing the output of converter 1 of the IPFC. In order to achieve the desired power flow in the primary line 1,converter 1 in the IPFC configuration injects an appropriate compensating voltage V_{1pq} to change the magnitude and angle of the line current I_1 , so as to force the flow of the desired real power P_1 and reactive power Q_1.It is seen from this phasor diagram that , from the standpoint of the primarily controlled line 1, the IPFC provides a two dimensional compensation capability for the independent control of the real line power P_1 and reactive power Q_1., similar to that obtainable with the UPFC.

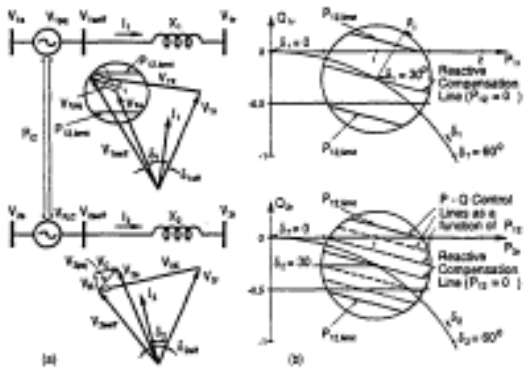

Figure.3. Phasor and Qr Vs P diagram illustrating the Operation of the elementary IPFC.

The two - dimensional voltage injection in series with line 1 generally results in the exchange of reactive power Q_{1pq} and of real power P_{1pq} between Line 1 and converter 1 of the IPFC. The reactive power Q_{1pq} exchanged is provided by converter1 itself, however. The real power P_{1pq} appears as a real power demand at its DC terminals. To satisfy this power demand , the control makes converter2 supply real power $P_{2pq} = - P_{1pq} = (\pm) P_{12}$ from line 2 to line 1 .In other words , converter 2 is controlled to regulate the common dc bus of the IPFC .This constraint of course means that the real power exchange for line 2 is pre-defined and therefore only its series reactive compensation can be freely varied to control the power flow in this line , in a manner done by controllable series reactive compensators such as the SSSC and TCSC.

The operation of converter2 is illustrated by the phasor diagram characterizing the simple, single line power system of line 2 in figure. The injected voltage of converter 2 is controlled with respect to the prevailing current in Line 2 to meet the real power demand of Line 1 and to provide the desired reactive series compensation for line 2. Accordingly, a voltage phasor component V_R, in phase (or anti-phase) with the line current phasor I_2, is injected with a magnitude to satisfy the real power demand of Line 1. Independent of voltage phasor component V_R, another freely controllable voltage phasor component Vq is injected in quadrature with I_2 to provide series reactive compensation. The sum of the injected in - phase and qudrature phasor components determine the injected voltage phasor of converter 2.

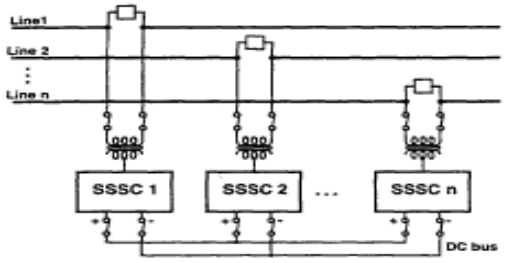

Figure.4. Multi line IPFC consisting of n SSSCs with a common dc link.

The IPFC configuration provides for series compensation, it is able to equalize not only the real power flow in a two-or multi line transmission systems, but also can equalize or control the reactive power flow in the lines. The IPFC provides an excellent tool to solve economically power flow problems in a multi line transmission system in which the actual power flows are not proportional to the capacities of the corresponding lines or to the desired power transmission in the individual lines, or in which the desired real power transmission in some lines is hindered by relatively high reactive power flow. The constraint for keeping the sum of the real power exchanged with n- lines zero can be circumvented by adding a shunt - connected converter the multi converter IPFC as illustrated in figure. This arrangement is particularly attractive in those cases in which the real power compensation requirement of the' weak' lines exceeds the real power that can be absorbed from the 'strong' lines without appreciably impacting their own power transmission is required anyway for voltage support.

3. STATIC SYNCHRONOUS SERIES COMPENSATOR (SSSC)

The concept of using the solid-state synchronous voltage source instead of a capacitor for series reactive compensation is based on the fact that the impedance versus frequency characteristic of the conventionally employed series capacitor, in contrast to filter applications, plays on part in accomplishing the desired line compensation. The function of the series capacitor is as illustrated in figure, to produce an appropriate voltage across the inductive line impedance and, thereby, the fundamental line current and the transmitted power. Therefore, if an AC voltage source of fundamental frequency, which is locked with a quadrature (lagging) relationship to the line current and whose amplitude is made proportional to that of the line current, is injected in series with the line, a series capacitor at the fundamental frequency is obtained. However, in contrast to the real series capacitor, the SVS is also able to maintain a constant compensating voltage in face of variable line current, or control the amplitude of the injected compensating voltage independent of the amplitude of the line current.

For normal capacitive compensation, the output voltage lags the line current by 90 degrees. However, the output voltage of the SVS can be reversed by simple control action to make it lead the line current by 90 degrees. In this case, the injected voltage decrease the voltage across the inductive line impedance and thus the series compensation has the same effect as if the reactive line impedance was increased. The series reactive compensation scheme employing an SVS, as illustrated in Figure, is termed the Static Synchronous Series Compensator (SSSC). The normalized power P versus and angle δ plots as a parametric function of the injected voltage Vq are shown in Figure 4. Comparison of these plots to those shown in figure for the series capacitive impedance compensation clearly shows that the series capacitor increases the transmitted power by a fixed percentage of that transmitted by the uncompensated line at a given δ and, by contrast, the SSSC increases it by a fixed fraction of the maximum power transmittable by the uncompensated line, independent of δ, in the important operating range of $0 \leq \delta \leq \pi/2$. From the standpoint of practical applications, steady state flow control or stability improvements, the SSSC clearly has considerably wider control range then the controlled series capacitor of same MVA rating.

4. SIMULATION RESULTS

The simulation is done using matlab and the results are presented. Model of transmission line 1 is shown in Figure 4a. Scopes are connected to measure the sending end current, receiving end voltage and power. Output current and voltages are shown in Figure 4b.Real and reactive powers are shown in Figures 4c and 4d respectively.

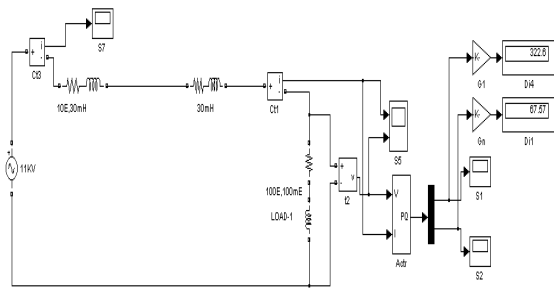

Figure.4a.Model of Single transmission line-1

Figure.4b.Output Current and voltage

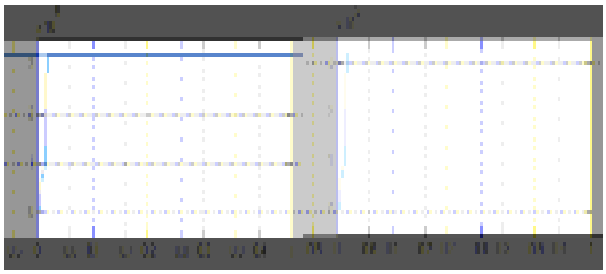

Figure.4c.Real power

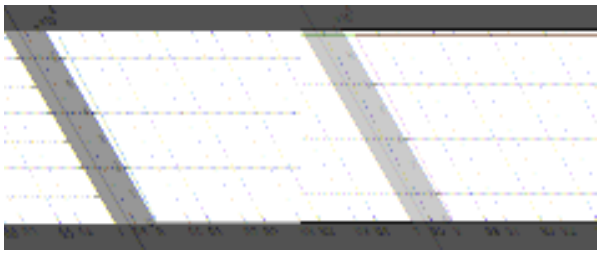

Figure.4d.Reactive power

Model of line 2 is shown in Figure 5a. The receiving end current and voltages are shown in Figure 5b.Real and reactive powers are shown in Figures 5c and 5d respectively.

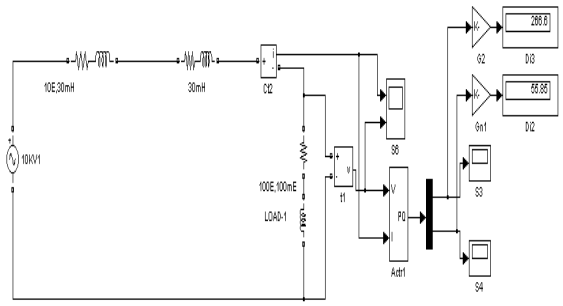

Figure.5a.Model of Single transmission line-2

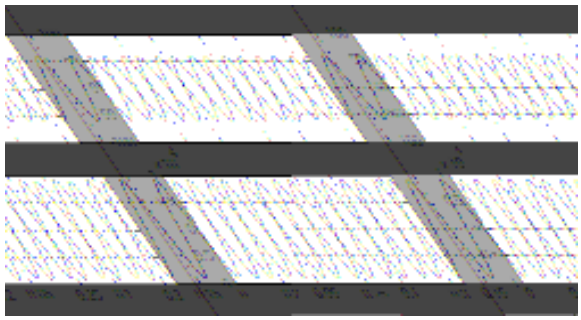

Figure.5b.Current and voltage output

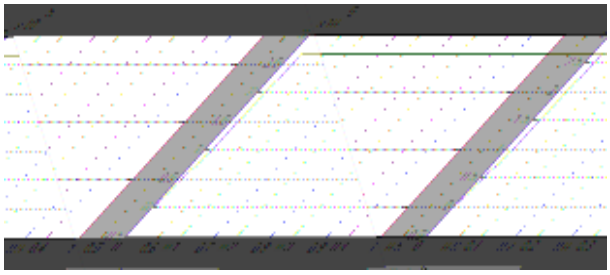

Figure.5c.Real power

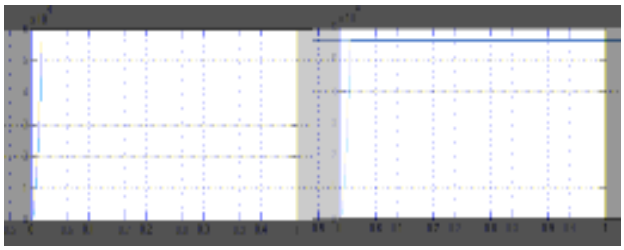

Figure.5d.Reactive power

Circuit with an additional load is shown in Figure 6a. Additional load is connected at t = 0.5 sec. It can be seen that the voltages decreases .The voltage across load 1 and load 2 are shown in Figure 6b.Reactive and real powers are shown in Figures 6c and 6d respectively.

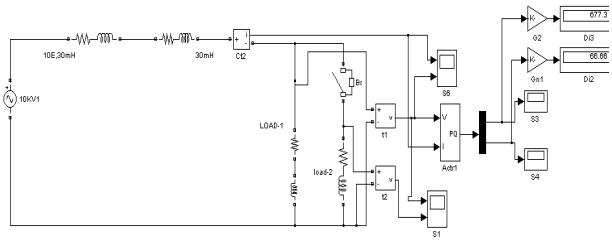

Figure.6a.Circuit diagram with sag condition

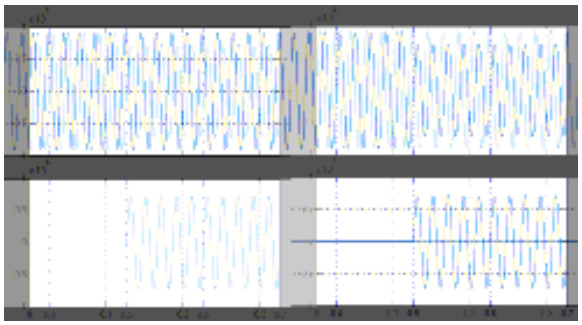

Figure.6b.Voltage across Load-1 and load-2

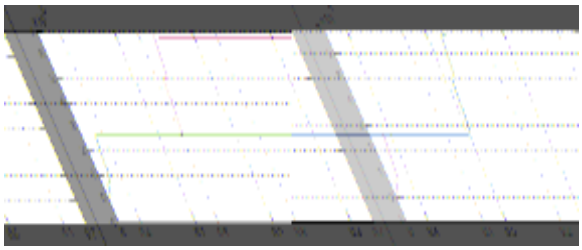

Figure.6c.Reactive power output

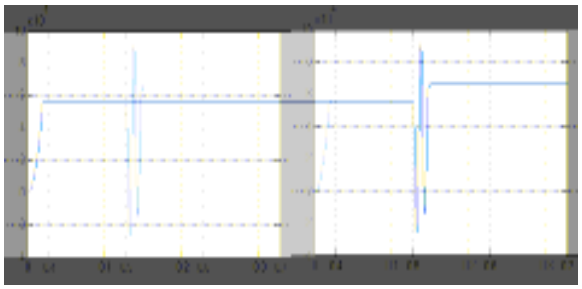

Figure.6d.Real power output

Four bus systems with IPFC is shown in Figure 7a. Current fed converter is shown in Figure 7b.Voltage across load 1, load 2 and IPFC are shown in Figure 7c. It can be seen that the IPFC is capable of mitigating the sag. Since the voltage decreases and comes back to normal value.

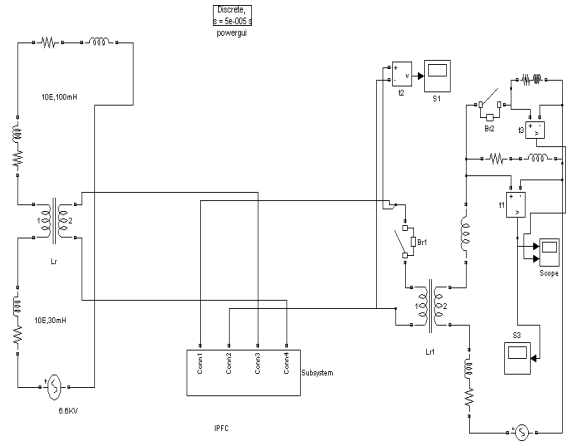

Figure.7a.Four bus system with IPFC

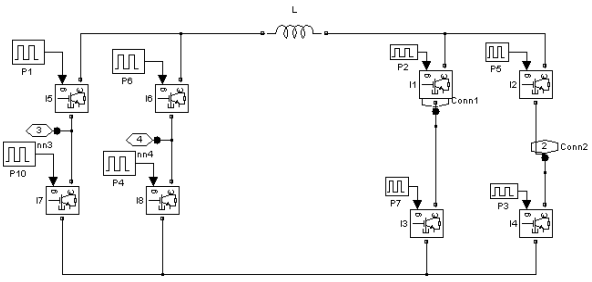

Figure.7b.Current fed IPFC system

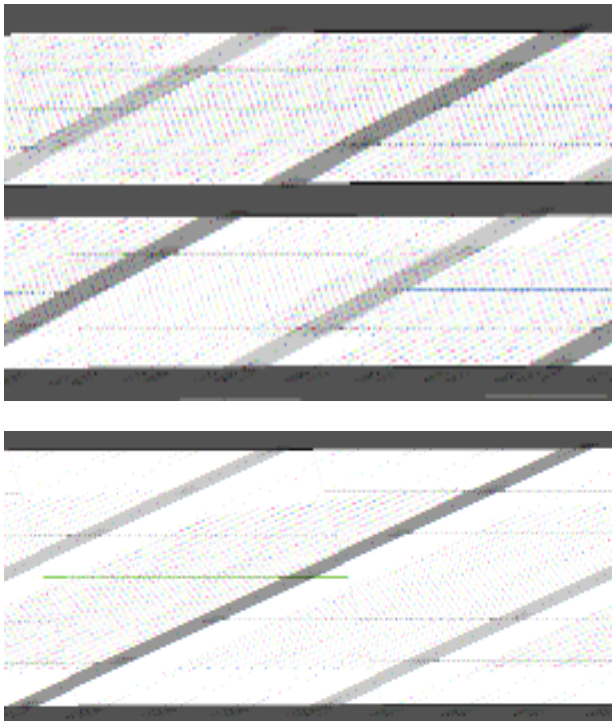

Figure.7c.Voltage across load -1, load- 2 and IPFC

5. CONCLUSION

Four bus system with and without IPFC are modeled and simulated using matlab simulink. Sag is created by connecting a heavy load across the existing load. The proposed current fed inverter is capable of mitigating the sag in the voltage .The simulation results are in line with the predicted results. Current fed IPFC is a viable alternative to the DVR for voltage sag mitigation. This work has considered balanced load. Single phase model is used for simulation studies.

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